SiC JFET Transistor in Current Limiting Regime and Short-Circuit Operation

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Abstract—This paper presents first destructive results showing the robustness of SiC JFET transistors from SiCED in current limitation regime or short-circuit operation. Crystal temperature during failure was estimated after different electrical characterisations and using appropriate models. For this purpose, the saturation current value has been linked to the temperature. Saturation current could be obtained over a wide temperature range (from 25 to 500°C) by extrapolating results of characterization to high room temperature (350°C) and using thermal model results. This work shows the exceptional robustness of JFET SiC transistors in current limitation mode compared to Si devices (MOSFETS and IGBTs).

Index Terms—JFETs, Silicon carbide, short circuit current

I. INTRODUCTION

In this paper we will present different characterization results, and destructive tests showing the exceptional robustness in short-circuit mode (current limiter) of SiC JFET transistors (1200V-15A in a TO220 package). These severe modes of operations result in a very fast increase in temperature of the chip which can lead to failure. It has been already shown that for Si devices failure appears during long short-circuit operations after thermal runaway and an energy density dissipated in the chip around 1 J/cm² [1]. One objective of this study is to evaluate the temperature of SiC crystal during the failure process. For this purpose, the saturation current is linked to the temperature of the crystal using experimental and 1D simulation results.

II. CHARACTERIZATION IN SHORT-CIRCUIT MODE

A. Description of the test bench

In order to characterize JFET transistors in current limitation mode (or short-circuit mode), a dedicated electric test bench was developed. Device under test (DUT) is used as a current limiting device and is maintained in the on-state (V_{GS} = 0V). A COOLMOS™ transistor in series with the DUT can set the duration of the current pulses T_{SC}. For long current pulses when failure appears, current is not limited any more and when it exceeds I_{ref} (arbitrarily fixed at 100A), COOLMOS™ transistor is open in order to avoid DUT Explosion. In order to characterize the saturation current dependence with temperature, DUT is placed in a stream of hot air (temperature controlled between 25°C and 350°C).

B. Characterization Results

Several studies have already shown the good behavior of SiC JFET transistors at high temperature and their potential as current limiter utilization [2-5]. Variation of the saturation current has been characterized for a wide temperature range from 25°C to 350°C. A low short-circuit duration of 6µs was chosen in order to limit the chip heating and to avoid any risk of failure. Results are presented on Fig.2, where we can see that SiC JFET transistors are able to ensure a current limitation regime (or to support a short-circuit mode) for an extremely high ambient temperature (350°C). The variation of the carrier mobility in the channel explains the strong variation of the saturation current with the temperature [4].

 III. 1D THERMAL MODEL

A. Description of the model

The power dissipated during a short-circuit phase is modelled by a power injection in the active area of top layer of the chip. The low duration (6µs) of the experimental short-circuit operation limits the vertical and horizontal diffusion of heat in the chip. Because the low horizontal diffusion of the heat, we considered only a 1D model. Due to the low vertical diffusion of the heat, only the chip (with its aluminium metallization) was modelled. In these conditions, we could not
take into account the effect of the bond wires that act locally like heat remover. In order to simplify, we assume as boundary condition on the upper chip area the power density obtained in the experiments described above (dissipated power divided by the active area) for each case temperature between 25 °C and 300 °C. Geometric parameters of the tested SiC JFET dies are summarized in table 1 and thermal properties of SiC material in table 2.

<table>
<thead>
<tr>
<th>Table 1: Characteristics of 1200V 15A SiC JFET Dies</th>
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<td>SiC thickness (µm)</td>
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<td>380</td>
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<th>Table 2: Thermal Properties of SiC [6]</th>
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<tr>
<td>Thermal properties</td>
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<td>---------------------</td>
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<tr>
<td>Conductivity (W.m⁻¹.K⁻¹)</td>
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<tr>
<td>Specific heat (J.kg⁻¹.K⁻¹)</td>
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<tr>
<td>Density (kg.m⁻³)</td>
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Due to the too large temperature variations, we didn't take into account the effect of the temperature on the thermal properties of Al metallization layer. The following data were used: $\lambda = 160 \text{ W.m}^{-1}\text{K}^{-1}$, $c = 900 \text{ J.kg}^{-1}\text{K}^{-1}$, $\rho = 2700 \text{ kg.m}^{-3}$.

We applied on the chip the following boundary conditions: power injection on the active area, adiabatic conditions at the edges and in the top surface of Al layer and isothermal conditions on the back face of the chip. This last simplification is justified only by the very low duration of the short-circuit process which limits the heat diffusion inside the crystal.

IV. INTERPRETATIONS

For each experimental result obtained between 25°C and 350°C and shown in Fig.2, we simulated the increase of the temperature in the SiC crystal. For example, simulation results give a maximum temperature calculated at the end of the short-circuit operation of about 304 °C in the SiC crystal for ambient temperature of 25°C (cf Fig. 3).

We can see from Fig.4 that the short-circuit current obtained at temperature of 25 °C, 6µs after the initiation of the short-circuit phase, corresponds to the levels of current reached at the beginning of short-circuit for room temperatures ranging between 300 and 350°C. This good agreement can validate the results obtained from thermal modelling.

The over current observed at the beginning of short-circuit current phase (partly due to the discharge of the output capacitance of the JFET) complicates the direct correlation between current and temperature at any beginning of short-circuit phase. However, from the various experimental results, and in a purely qualitative way, by directly connecting the temperature to the maximum value of the current obtained at the beginning of short-circuit phase, we can compare this estimation of the crystal temperature with the simulations results.

Figure (5) Comparison between thermal simulation results and temperature estimated from saturation current (temperature simulated for a short-circuit with room temperature of 25°C and $E = 400$ V).
Results show a good agreement between temperature estimated from saturation current and simulated temperature thus justifying the use of the saturation current as an indicator of temperature at the hottest spot of the crystal, for the whole temperature range. Results are shown on Fig.6.

Figure (6) Saturation current according to the temperature (E = 400V).

The theoretical variation of the saturation current with the temperature level: \( I_{sat}(T) = I_{sat}(300K) \cdot (T/300)^{2/4} \) [ref], related to the influence of the carriers mobility isn’t satisfactory. So, we used the following simplified mathematical model which has been found more well-suited: \( I_{sat} = I_{sat0} \cdot \exp(-\theta_0/\theta_0) \), where \( \theta \) is temperature (in °C), \( I_{sat0} = 50 \) A and \( \theta_0 = 384 \) °C. This relation is drawn in Fig.7 and compared with experimental estimations for a temperature range between 100 °C and 500 °C.

Figure (7) Model of saturation current with temperature (E = 400V).

The failure appears after 660µs which corresponds here to an energy of 2.4 J, approximately 60 J/cm² in the active area, much more than that measured on silicon devices.

From this last result, we can use the saturation current as a thermal indicator in order to estimate the temperature value inside the crystal during this short-circuit process. Especially, we can assess the temperature reached at the end of the short-circuit (Fig.9).

The maximum estimated temperature is higher than the melting temperature of aluminum (metallization), but still below the critical temperature of SiC for this level of voltage, suggesting that the failure is certainly related to the environment of the die (packaging, metallization, passivations...).

Figure (8) Destructive test (E = 400V T_{CASE} = 25°C).

Figure (9) Estimation of the temperature during a long term short circuit phase (E = 400V T_{CASE} = 25°C).

VI. CONCLUSION

The article presents an experimental study of the behaviour of SiC JFET transistors in current limitation mode. We thus could show the exceptional robustness of these components to the modes of short-circuits. The results show the exceptional strength of transistors JFET SiC compared to silicon transistors, which offers extremely interesting possibilities in terms of series protection.
REFERENCES


